In the Claims:

Following is a complete listing of the claims pending in the application, as amended:

1-47. (Cancelled)

48. (Currently amended) A process of electrically coupling a ~~microelectronic component~~ semiconductor die having an integrated circuit to a substrate, comprising:

forming a ~~plurality of~~ multi-layer bond ~~pads~~ pad by:

depositing an intermediate bond layer of a first metal on an outer surface ~~of each of a plurality~~ of an integrated bond ~~pads~~pad carried by ~~an active~~a first surface of the ~~microelectronic component~~semiconductor die, the integrated bond ~~pads~~ pad and the integrated circuit being formed of a second metal selected from the group consisting of aluminum and copper~~different from the first metal~~; and

thereafter, depositing an outer bond layer on the intermediate bond layer ~~deposited on each integrated bond pad~~, the outer bond layer comprising a ~~second metal~~ third metal, which is different from the first metal and the second metal;

~~thereafter,~~ positioning the microelectronic component with respect to the substrate with the ~~active~~ first surface of the microelectronic component spaced from a contact surface of the substrate;

ball bonding a first end of a ~~first~~ bonding wire to a ~~first~~ contact carried by the contact surface of the substrate, the ~~first~~ bonding wire comprising the ~~first~~ third metal; and

stitch bonding a second end of the ~~first~~ bonding wire to the outer bond layer of ~~a first one of~~ the multi-layer bond ~~pads~~pad.

49. (Currently amended) The ~~method~~ process of claim 48 wherein the ~~first~~ third metal comprises gold.

50. (Currently amended) The ~~method~~ process of claim 48 wherein the outer bond layer is electrodeposited.

51. (Currently amended) The ~~method~~ process of claim 48 wherein the integrated bond pad is a first integrated bond pad, the multi-layer bond pad is a first multi-layer bond pad and the bonding wire is a first bonding wire, the process further comprising forming a second multi-layer bond pad, ball bonding a first end of a second bonding wire to a second contact carried by the contact surface, and stitch bonding a second end of the second bonding wire to the outer bond layer of ~~a~~ the second ~~one of the~~ multi-layer bond ~~pads~~pad.

52. (New) The process of claim 48 wherein the first metal comprises titanium, tungsten, chromium, or an alloy of titanium, tungsten, or chromium.

53. (New) The process of claim 48 wherein an outer surface of the outer bond layer is spaced no more than 1 μm from the integrated bond pad.

54. (New) The process of claim 48 wherein the substrate comprises a flexible substrate.

55. (New) The process of claim 48 wherein the integrated bond pad has an effective surface area, the outer bond layer having an outer surface with a surface area that is no less than the effective surface area of the integrated bond pad.

56. (New) The process of claim 48 further comprising depositing an abrasion-resistant passivation layer on the first surface of the die.

57. (New) The process of claim 48 wherein the semiconductor die includes an abrasion-resistant passivation layer having a passivation opening aligned with the integrated bond pad and the outer bond layer extends laterally outwardly beyond a periphery of the passivation opening with which the bond pad is aligned.

58. (New) The process of claim 48 wherein the bonding wire has a maximum height of no greater than 3 mils outwardly from the first surface of the die.

59. (New) A process of electrically coupling a microelectronic component to a substrate, comprising:

forming a multi-layer bond pad by:

depositing a passivation layer on a first surface of the microelectronic component, the first surface carrying an integrated bond pad that has a surface area and is formed of a first metal, wherein an effective surface area of the integrated bond pad, which is less than the surface area of the integrated bond pad, is exposed by an opening of the passivation layer;

depositing an intermediate bond layer of a second metal on the effective surface area of the integrated bond pad; and

depositing an outer bond layer on the intermediate bond layer, the outer bond layer comprising a third metal that differs from the first metal;

positioning the microelectronic component with respect to the substrate with the first surface of the microelectronic component spaced from a contact surface of the substrate;

ball bonding a first end of a bonding wire to a contact carried by the contact surface of the substrate, the bonding wire comprising the third metal; and

stitch bonding a second end of the bonding wire to the outer bond layer of the multi-layer bond pad.

60. (New) The process of claim 59 wherein the first metal comprises aluminum.

61. (New) The process of claim 59 wherein the second metal comprises a metal selected from a group consisting of titanium, tungsten, and chromium.

62. (New) The process of claim 59 wherein the third metal comprises gold.

63. (New) The process of claim 59 wherein the first metal comprises copper or aluminum and the third metal comprises gold.

64. (New) The process of claim 59 wherein the third metal comprises copper.

65. (New) The process of claim 59 wherein the outer bond layer is electrodeposited.

66. (New) The process of claim 59 wherein the passivation layer is silicon nitride.

67. (New) The process of claim 59 wherein the passivation layer is a moisture barrier.

68. (New) The process of claim 59 wherein the multi-layer bond pad is a first multi-layer bond pad and the bonding wire is a first bonding wire, further comprising forming a second multi-layer bond pad, ball bonding a first end of a second bonding wire to a second contact carried by the contact surface, and stitch bonding a second end of the second bonding wire to the outer bond layer of the second multi-layer bond pad.

69. (New) The process of claim 59 wherein the periphery of the intermediate bond layer extends beyond the periphery of the opening in the passivation layer.

70. (New) The process of claim 59 wherein the periphery of the outer bond layer extends beyond the periphery of the opening in the passivation layer.

71. (New) A process of electrically coupling a microelectronic component to a substrate, comprising:

forming first and second multi-layer bond pads by:

depositing an intermediate bond layer of a first metal on a first surface of a microelectronic component, the first surface carrying first and second bond pads that each comprise a second metal;

depositing a process layer having a first opening associated with the first bond pad and a second opening associated with the second bond pad;

depositing an outer bond layer of a third metal on the intermediate bond layer in each of the first and second openings; and

removing the process layer;

attaching the microelectronic component to the substrate with the first surface of the microelectronic component spaced from a contact surface of the substrate;

ball bonding a first end of a bonding wire to a contact carried by the contact surface of a substrate, the bonding wire comprising the third metal; and

stitch bonding a second end of the bonding wire to the outer bond layer of the first multi-layer bond pad.

72. (New) The process of claim 71 wherein the second metal comprises a metal selected from a group consisting of titanium, tungsten, and chromium.

73. (New) The process of claim 71 wherein the first metal comprises aluminum or copper.

74. (New) The process of claim 71 wherein the third metal comprises gold.

75. (New) The process of claim 71 wherein the third metal comprises copper.

76. (New) The process of claim 71 wherein the outer bond layer is electrodeposited.

77. (New) The process of claim 71 further comprising ball bonding a first end of a second bonding wire to a second contact carried by the contact surface and stitch bonding a second end of the second bonding wire to the outer bond layer of the second multi-layer bond pad.

78. (New) A process of electrically coupling a microelectronic component to a substrate, the microelectronic component having an integrated circuit and an integrated bond pad, both of which comprise a first metal selected from a group consisting of copper and aluminum, the process comprising:

forming a multi-layer bond pad by:

depositing an intermediate bond layer of a second metal on an outer surface of the integrated bond pad, the second metal being selected from a group consisting of titanium, tungsten, and chromium; and

depositing an outer bond layer comprising gold on the intermediate bond layer;

attaching the microelectronic component to the substrate with the first surface of the microelectronic component spaced from a contact surface of the substrate;

ball bonding a first end of a bonding wire to a contact carried by the contact surface of the substrate, the bonding wire comprising gold; and

stitch bonding a second end of the bonding wire to the outer bond layer of the multi-layer bond pad.